AMENDMENTS TO THE SPECIFICATION:

Page 8, please amend the paragraph beginning at line 25 and continuing to page 9, line 12 as follows:

Figure 4 is a flow diagram schematically illustrating a testing methodology for the system of Figure 2. At step 20 a test pattern is loaded using a serial scan chain (such as the wrapper scan chain) to test the processor core 2 and those memory port connections 8 which are provided with scan chain cells, e.g. high order address bits of the memory access port connecting to the optional memory. The memory size signals are also toggled during this testing to check these signals. The memory port connections with scan cells are tested by driving signals out of the processor core 2 for capture in the scan chain cells 10 under the test pattern control. Step 22 serves to determine whether or not this phase of the testing is passed. If the test is not passed, then processing proceeds to step 23 at which the component is failed. If the check for a pass at step 22 is successful, then processing proceeds to step 24 at which an appropriate test pattern is driven into the processor core 2 to test the remaining memory access port connections (if a memory is actually connected) by driving signals out of the processor core 2, through the memory 4 and back into the processor core 2 under test pattern control. Whilst this testing is taking place the memory size signals are set to have values such that the memory (if present) is taken to have the smallest non-zero supported memory size. Step 26 then determines whether or not this test has been passed. If the test has not been passed, then the component is again failed at step ~~24~~23. If the test at step 26 indicates a pass of the

second phase of the testing, then processing proceeds to step 28 at which the component concerned is passed and maybe released for use. If an optional memory is not present the steps 24 and 26 can be omitted.